ACOUSTICS 2012

Research & Medical Doppler platform

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A new ultrasound digital transcranial Doppler system (digiTDS) is introduced. The digiTDS enables diagnosis of intracranial vessels which are difficult to penetrate for standard systems. The device can display a color map of flow velocities in time-depth domain and a spectrogram of a Doppler signal received from a particular depth. The system offers a multigate processing that allows to display simultaneously a number of spectrograms and to reconstruct a flow velocity profile.

The digital signal processing in digiTDS is partitioned between hardware and software parts. The hardware part (based on FPGA) executes a signal demodulation and reduces data stream. The software part (PC) performs the Doppler processing and display tasks. The hardware-software partitioning allowed to build a flexible Doppler platform at a relatively low cost.

The digiTDS design fulfills all necessary medical standards being a new useful tool in transcranial field as well as in heart velocimetry research.

1 Introduction

Ultrasound Doppler techniques are diagnostic tools which are implemented in a rapidly growing number of medical devices. However, due to specific conditions of transcranial examinations most of devices offer results of poor quality. Only a few systems are dedicated to the transcranial diagnosis.

RIMED Digi-Lite [13] (RIMED, Israel) is a dual channel transcranial Doppler (TCD) system with an advanced and proprietary M-Mode Display. The system has a complete range of probes: 2 MHz, 4 MHz, 8 MHz and 16 MHz, each with a separate connector. The 2 MHz probe can insonify the brain in 64 different depths/gates at the same time, displaying 8 different Doppler spectrum windows simultaneously. Its high sensitivity enables detection of flow velocity at the contra-lateral side of the brain. It offers an optional imaging probe for complete and accurate color-coded ultrasound scanning of the Carotid System.

SONARA TCD System [14] (SONARA, USA) allows the TCD exams to be performed quickly and efficiently utilizing M-Mode for 250 gates. The system is available in unilateral and bilateral configuration and gives access to patient files in multiple export formats including raw data.

DWL Multi-Dop X Digital [15] (Compumedics, Germany) is a dual channel Doppler system with 400 gates of M-Mode display and 4 spectrum windows. It can operate in both pulse and continuous wave modes in the frequency range of 1 to 16 MHz and gives access to raw data.

The model example of combined ultrasound system architecture is a Doppler device introduced in [11]. The module designed by Ricci et al. is composed of a FPGA (Altera® Stratix) executing hardware processing functions, and a DSP (Texas Instruments® TMS320C67). The module communicates with a PC and is responsible for the control and display functions through the USB interface. The quadrature demodulator, a set of digital filters and a decimator have been implemented in the FPGA. The initially demodulated and decimated data stream is transferred to the DSP, executing standard Doppler algorithms. The system is similar to commercial solutions in terms of the construction, however it is intended for researchers only.

The main purpose of our work was to build a device which would serve in both research labs and clinics. DigiTDS introduced in this paper fulfills all necessary medical requirements to be approved for medical use.

The basic design of the digiTDS is similar to that of Ricci et al. Both systems are based on a mixed model of hardware-software signal processing [3]. The acquisition of the RF echo signal are based on a fast A/D converter and a FPGA, being an interface to the further part of the system. The application of the FPGA at the beginning of the digital channels is now a standard solution. Apart from signal acquisition, the FPGA most often executes hardware processing of a digital signal. The aim of this is to reduce the data stream for further processing [6]. Next, the processing is executed by DSP, GPP, GPU or combinations of these processors [5].

2 Transcranial Doppler system

The pulse wave Doppler method allowing to measure the flow at a selected depth is a standard for intracranial diagnostic device. The current diagnostic solutions are mainly focused on a complex assessment and a monitoring of cerebrovascular flow in different pathological conditions, especially those which potentially affect normal functioning of the central nervous system.

The digiTDS device (Fig. 1) is a multigate transcranial Doppler system [9]. This system is composed of two electronic modules of 130 mm × 82 mm dimensions responsible for ultrasonic signal transmission, acquisition and demodulation, and a PC responsible for Doppler signal processing after demodulation and for data presentation.

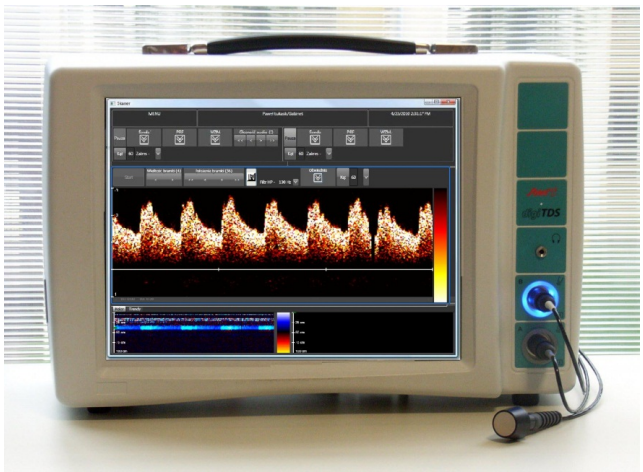

Figure 1: The digiTDS system.

The system block scheme is shown in Fig. 2. On the analogue-digital module board, there are two independent transmission-reception channels (the device supports simultaneous operation with two probes in bilateral operation mode). A 10-bit DAC (Texas Instruments® DAC5652A) operating at a speed of 64 MSPS is used to generate the transmitted signal.

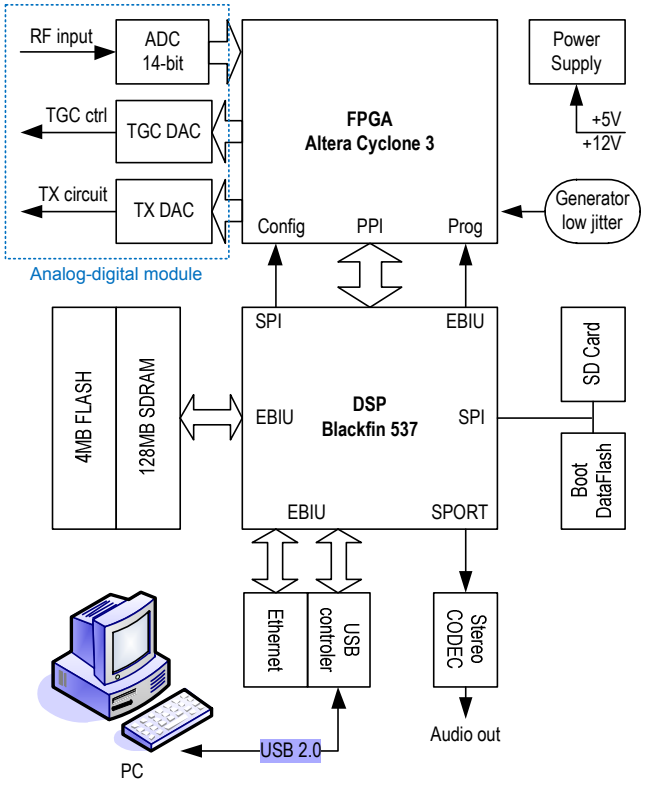

Figure 2: Simplified block diagram of the digiTDS system.

The reception track contains amplifiers including time gain compensation TGC (Analog Devices® AD8331) and a dual 14-bit ADC (Analog Devices® AD9640) with sampling frequency of 64 MHz. The digital signals from/to ADC are connected to the FPGA on the digital module board via inter module connector. The digital module consists of the FPGA (Altera® Cyclone 3 EP3C25), the DSP (Analog Devices® Blackfin BF537) as well as USB device controller (PLX® NET2272) and an Ethernet interface. The digiTDS communicates with the PC via USB 2.0 interface. However, it can run independently of the PC, due to its own control resources - the DSP processor.

3 Digital signal processing

The digital processing chain consists of hardware processing in the FPGA and software processing using the DSP and the PC's CPU. The application of hardware resources during early processing stage allowed to significantly decrease the required data throughput and the computing load of the PC [10]. It also allowed to use a low-power single-board PC with Intel® ATOM processor and to extend the operating time on batteries. The distribution and implementation of processing tasks were performed and tested on a constructed prototype device. Especially, shifting the filtration in multiple gates from software to the FPGA gave significant time savings of the processor. Fig. 3a presents the track of the Doppler digital signal processing on the digiTDS device with task distribution between the FPGA system and the software.

3.1 Preprocessing - the FPGA

The data path of the implemented FPGA logic (Fig. 4) consists of three components: a quadrature demodulator (DDC - Digital Down Converter), a decimator (integrated into a CIC filter Cascaded Integrator Comb) and a set of wall filters.

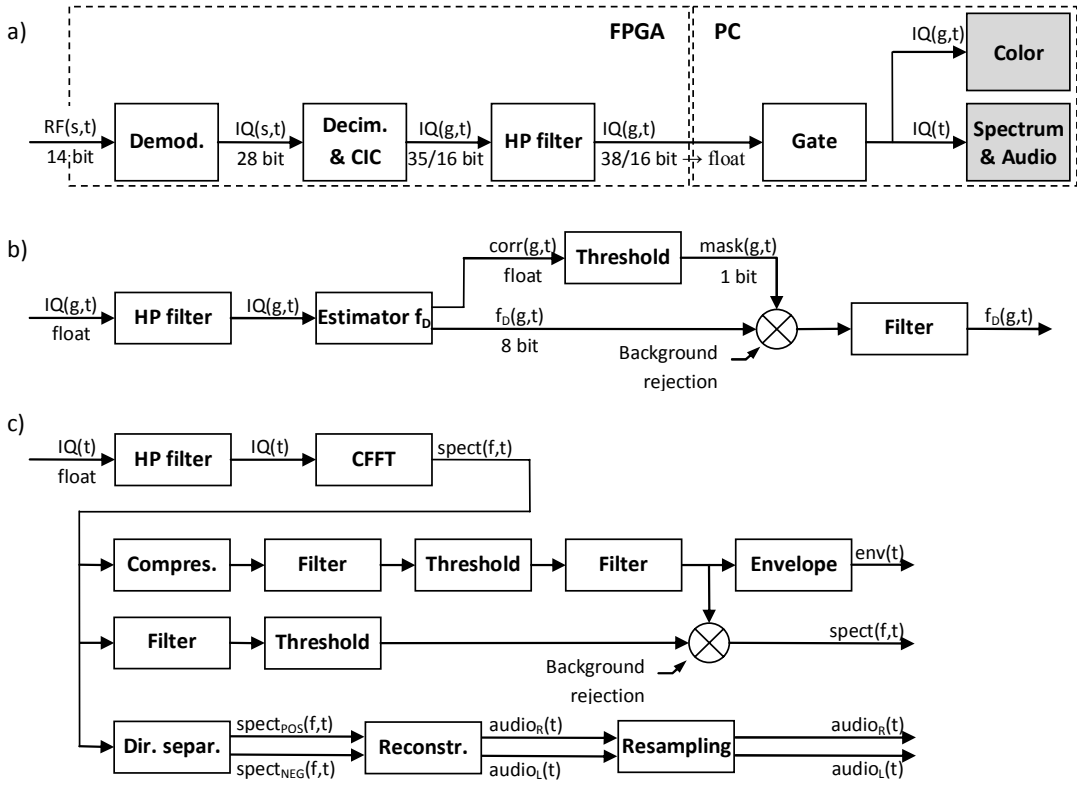

Figure 3: The Doppler digital signal processing scheme: a) preprocessing, b) color chain, c) spectrum and audio chain.

The DDC employs a quadratic demodulation to convert the received radio frequency real signal (RF) to a complex signal (I/Q - in phase/quadrature) centered at zero frequency baseband. The resulting quadrature I/Q signal enables to separate easily the flow directions in further processing.

The DDC accepts 14-bit RF echo signal samples in two's complement format at its input port and produces a pair of 28-bit down-converted I/Q signals at its output ports. The demodulator is composed of two multipliers, six memories containing reference signals and two multiplexers. Each of the memories contains one period of reference sine and cosine signals sampled at 64MHz with 14-bit resolution.

The two multipliers were implemented as Altera IP lpm_mult components. The first input port of the multipliers is directly connected to the input port of the demodulator, the second is connected via 3-to-1 multiplexer to the memory containing reference signal samples. It gives a choice of selecting one of three demodulation frequencies. Output ports of the multipliers are directly connected to the output ports of the demodulator.

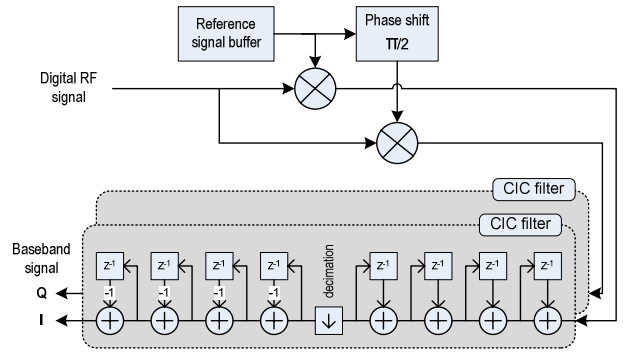

Figure 4: The block diagram of the digital quadrature demodulator with CIC filter implemented in the FPGA.

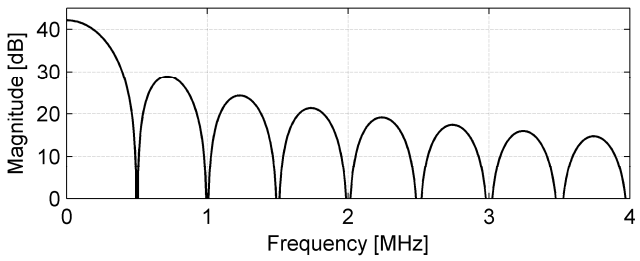

Figure 5: The impulse response of the CIC filter for the decimation factor value set to 128. The sampling frequency is 64 MHz. The zeros of the filter frequency response are related to the frequencies which would alias directly into the required baseband.

The I/Q signal is next passed on to a CIC [8], (Cascaded Integrator Comb) filter which is a finite impulse response low-pass filter dedicated for decimation It performs both: anti-aliasing filtration and decimation. In comparison to standard FIR filters it offers frequency response (Fig. 5) which is well-matched for decimation purposes for relatively low computation cost [7].

Each CIC filter accepts 28-bit down-converted RF echo signal samples at its input port and produces 35-bit decimated baseband signal at its output port. The CIC filter is composed of a recursive integrator, a decimator and a differentiator. The decimation factor is run-time programmable thus it enables controlling the Doppler gate size. In a typical transcranial operation mode the decimation factor value is set to 128 which gives the Doppler gate size of 2 μs (1.5 mm) and reduces the data rate from 64 MSPS to 0.5 MSPS.

The 35-bit output of the CIC filter is passed through a Gain and Saturation block that selects 16 bits for further processing. Next the signal is transfered into a wall filter.

The wall filter is a high-pass filter which is intended to suppress low-frequency signals related to a stationary tissue (e.g. vessel's walls - hence the name). The wall filter implemented in the FPGA performs only an initial filtration. It allows to reduce complexity of the next stage wall filters which are implemented on the PC.

The choice of the wall filter structure was made with respect to various aspects. An IIR structure offers good frequency response for low computation costs. However, when fed with input signals of high amplitude, it can become unstable. Employment of the IIR filter would force to limit the dynamic range of the input signal, which is highly undesirable. Finally, a FIR filter type was chosen due to its unconditional stability.

From the functional viewpoint the wall filter component is composed of 200 FIR filters (two for each of 100 gates, one for I and one for Q data), each with the length of 64 run-time programmable coefficients. This filter bank operates in a fully serial manner, which means that it performs one multiply-accumulate operation per clock cycle and it takes 64 clock cycles to filter one Doppler gate.

From the structural viewpoint the wall filter is composed of a memory bank containing FIR filter states, a memory containing FIR filter coefficients, two multipliers and two accumulators. In order to optimally use the FPGA memory resources the filter states memory bank was implemented as 25 Altera IP altsyncram components each in a 256 words by 32 bits configuration, and the filter coefficients memory was implemented as a single altsyncram component in a 64 words by 16 bits configuration. The multipliers were implemented as 16-bit Altera IP lpm_mult components whereas the accumulators were implemented as 38-bit Altera IP altaccumulate components. They perform together a single multiply-accumulate operation separate for the I and Q channels. The wall filter output ports are connected to the final data path multiplexer via the Gain and Saturation block which selects 16 out of 38 bits for further software processing.

The cumulative utilization of logical resources of the applied FPGA (Altera® EP3C25) amounted to 43% of logic cells, 79% of internal block RAM and 12% of dedicated 18-bit multipliers. Time closure was obtained for the frequency of 64 MHz, and thus the processing speed matched the speed of input data stream (RF signal sampling).

Afterwards the processed signal is sent to the PC where it is processed specifically for a given application including color flow mapping (Color) and Doppler spectral analysis (Spectrum). The Color mode display allows the operator to find easily a preferred blood vessel and apply the Spectrum mode which enables a complete analysis of the flow vascular conditions.

3.2 Color channel

The processing in the Color channel (Fig. 3b) starts with the final wall filter which removes the residual remains of clutter echoes after the initial wall filtration executed in the FPGA. A mean frequency estimation which follows the filtration, is heavily sensitive to low frequency clutter. Thus, an additional rejection of the clutter is crucial for the whole Color chain to work correctly [1,4].

Afterwards the signal is passed to the autocorrelation-based mean frequency estimator [12]. The results depend on time and depth therefore they can be used to form a 2D map of Doppler frequencies.

However, such a map (Fig. 6b) pictures not only the flow of blood but it also contains a random noisy background which has to be eliminated. To reject the unwanted part of the map of frequencies we use an adaptive background rejection algorithm which employs a map of autocorrelation (AC) factor values (Fig. 6a). This map is generated in the process of mean frequency estimation, so no additional computations are required. The autocorrelation factor behaves similarly to the Doppler power factor. In fact, the power is commonly used for the background rejection. However, we observed that the autocorrelation factor allows the adaptive background rejection algorithm to perform more efficiently, so it is the another part of the Color chain for improved performance.

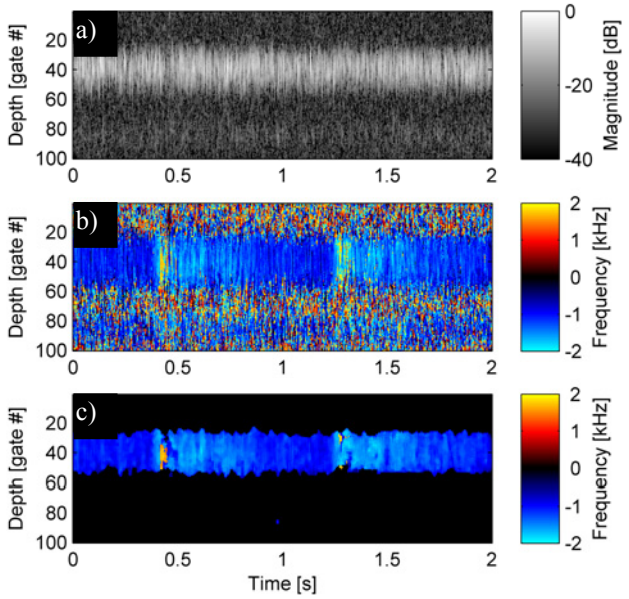

Figure 6: a) the raw AC map, b) the raw map of Doppler frequencies, c) the map of Doppler frequencies after the background rejection.

The map of Doppler frequencies after the background rejection and final filtration is ready to be displayed in a color scale (Fig. 6c).

3.3 Spectrum channel

The Spectrum channel (Fig. 3c) enables an audio-visual presentation of the Doppler data from a selected depth (gate). Actually, the audio output allows only a qualitative analysis and it does not provide additional information to those introduced by visual display. Nevertheless, it is still a useful tool which improves perception of the data [1].

The Audio part of the Spectrum channel could pass the Doppler data straight to a sound card as the signal is in the acoustic band already. However, a distinction of directions of the blood-flows requires additional operations. The so called direction separation can be performed in several ways [2]. The digiTDS employs a separation in frequency domain. This method starts with a Fast Fourier Transform (FFT) of the complex IQ signal. The produced series of spectra are split into two channels containing positive and negative frequencies which represent flows directed towards and away from a probe respectively. Next, the separated spectra are back-transformed (inverse FFT) to the time domain, assembled into two continuous audio-tracks, passed to the sound card and played in stereo mode.

The Spectrogram part of the Spectrum channel also starts with the FFT producing a series of spectra which are formed into the spectrogram (Fig. 7a). However, the result is noisy and difficult for automated analysis. Therefore, the background rejection algorithm is applied. The resulting image (Fig. 7b) is smooth and devoid of background, hence it is more readable and better for further analysis. The final step is to derive an envelope of the spectrogram, which corresponds to maximal flow velocity as a function of time.

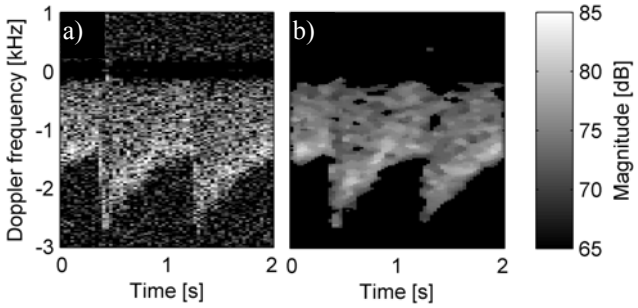

Figure 7: The spectrograms: a) raw, b) after the background removal.

Furthermore, our system provides multi-gate processing which allows to observe and analyze the spectrograms at many different gates simultaneously. This feature also enables the reconstruction of a flow velocity profile in real time and opens the way for an implementation of ultrasonic velocimetry application (which is in progress).

4 Applications

Since the first application in 1982 Transcranial Doppler is accepted as a non-invasive method of viewing the blood flow in the cerebral (brain) arteries and veins. Being a diagnostic tool it can be used at bedside to assess the cerebral vasculature in inexpensive, safe and reliable way. It can be repeated multiple times or used for continuous monitoring if needed. Immediate, real time detection of changes in cerebrovascular hemodynamics is possible. It can be utilized by any medical specialty to evaluate several neurovascular disorders. The common Transcranial applications include: screening for intracranial diseases - MCA stem stenosis and occlusion, carotid siphon stenosis distal vertebral stenosis, basilar stenosis, collateral flow, vasospasms. Transcranial is a tool in the diagnosis of medical conditions such as cerebral emboli, stroke diagnosis and treatment as well as vasospasm related to a subarachnoid hemorrhage.

The intracranial arteries may be examined through conventional temporal, foraminal, and orbital windows. It is a "blind procedure": its accuracy relies on the knowledge and experience of a trained operator and interpreter. According to the literature, in 5% to 10% of cases, the sufficient penetration of the bone window cannot be achieved for ample insonation attributable to skull characteristics. Doppler is useful only if a reliable signal is found.

The digiTDS performance was tested on cases with identified „poor acoustic window". The ability of the system to obtain simultaneous signals from different vessels with the reduced acoustic power emission was considered and tested.

5 Conclusions

The paper presents the technical development of the new multigate Doppler device pertaining to the architecture of digital signal processing and task distribution between software and hardware in ultrasound diagnostic devices. The presented system offers standard Doppler modes (audio, spectrum and color), and thanks to its multigate processing it enables a reconstruction of a flow velocity profile and allows an implementation of ultrasonic velocimetry.

The experiences gained during designing and implementation of the digital processing algorithms on this platform show their unquestionable advantages, namely:

- possibility of the algorithm migration between hardware and software solutions,
- possibility of equalization of the load distribution in all system elements and the data transfer between sub-systems,
- possibility of optimization of the selected system parameters (time delay, data transfer, power consumption, etc.) by changing the method/place of processing execution.

The developed Doppler system is a unique combination of the research equipment and the certified medical device. Its mixed architecture allows for the implementation of the advanced signal processing while keeping the costs low. Further work will aim to implement methods for detection of microemboli at cardiological applications, and monitoring in assisting with the artificial heart ventricle.

Acknowledgments

Project POIG.01.03.01-14-012/08-00 co-financed by the European Regional Development Fund under the Innovative Economy Operational Programme.

INNOVATIVE ECONOMY
NATIONAL COHESION STRATEGY
EUROPEAN UNION
EUROPEAN REGIONAL DEVELOPMENT FUND

References

[1] M. Ali, D. Magee, U. Dasgupta, *Signal processing overview of ultrasound systems for medical imaging*, Texas Instruments, White Paper, SPRAB12, 2008

[2] N. Aydin, L. Fan, D. H. Evans, "Quadrature-to-directional format conversion of Doppler signals using digital methods", *Physiol. Meas.*, Vol. 15, pp. 181-199, 1994

[3] S. A. Bassam, M. M. Ebrahimi, A. Kwan, M. Helaoui, M. P. Aflaki, O. Hammi, M. Fattouche, F. M. Ghannouchi, "A generic architecture for smart multi-standard software defined radio systems", presented at the SDR'09 Technical Conference and Product Exposition, Washington, D.C., USA, December 1-4, 2009

[4] S. Bjaerum, H. Torp, "Statistical evaluation of clutter filters in color flow imaging", *Ultrasonics*, Vol. 38, pp. 376-380, 2000

[5] J. H. Chang, L. Sun, J.T. Yen, K. K. Shung, "Low-cost, high-speed back-end processing system for high-frequency ultrasound B-mode imaging", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 56, No. 7, 2009

[6] P. Garcia, K. Compton, M. Schulte, E. Blem, W. Fu, "An overview of reconfigurable hardware in embedded systems", *EURASIP Journal on Embedded Systems*, Volume 2006, Article ID 56320, 2006

[7] F. J. Harris, *Multirate signal processing for communication systems*, Prentice Hall PTR, ISBN 978-0131465114, 2004

[8] E. Hogenauer, "An economical class of digital filters for decimation and interpolation", *IEEE Transactions on Acoustics, Speech and Signal Processing*, Vol. 29, pp. 155-162, 1981

[9] M. Lewandowski, M. Walczak, A. Nowicki, "Compact modular Doppler system with digital RF processing", in Proceedings of IEEE International Ultrasonics Symposium, Roma, Italy, September 20-23, 2009, pp. 1848-1851

[10] J. H. Reed, *Software Radio: A modern approach to radio engineering*, Prentice Hall, ISBN 978-0130811585, 2002

[11] S. Ricci, A. Dallai, E. Boni, L. Bassi, F. Guidi, A. Cellai, P. Tortoli, "Embedded system for real-time digital processing of medical ultrasound Doppler signals", *EURASIP Journal on Advances in Signal Processing*, Volume 2008, Article ID 418235, 2008

[12] A. C. H. Yu, K. W. Johnston, R. S. C. Cobbold, "Frequency-based signal processing for ultrasound color flow imaging", *Canadian Acoustics*, Vol. 35, No. 2, pp. 11-23, 2007

[13] RIMED Digi-Lite documentation: http://www.rimed.com/site/down/RIMED005Catalogue%20v8%20by%20pages%20high%20resoultion.pdf

[14] SONARA TCD System documentation: http://www.viasyshealthcare.com/prod_serv/prodDetail.aspx?config=ps_prodDtl&prodID=158

[15] DWL Multi-Dop X Digital documentation: http://dwl.de/fixfoxdateien/pdf/DWL-datasheet_multi-dop-xdigital.pdf